

JEDEC STANDARD

**SON/QFN Package Pinouts Standardized
for 1-, 2-, and 3-Bit Logic Functions**

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS

(From JEDEC Board Ballot JCB-04-44, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to SON/QFN packaged 1-, 2- and 3-bit logic devices.

The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 6- or 8-land SON/QFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Terms and definitions (for the purpose of this document)

DIP: Dual In-line Pin Package (gull-wing)

SOP: Small-Outline Package; 0.95-mm lead pitch; 1.6mm wide body (MO-178; variations AA (5-ld), AB (6-ld), and BA (8-ld)).

SSOP: Shrink Small-Outline Package; 0.65-mm lead pitch; 5.3-mm wide body (MO-150; variation AA (8-ld)).

TSSOP: Thin Shrink Small-Outline Package; 0.65-mm lead pitch; 4.4-mm wide body (MO-153; variation AA (8-ld)).

SON: Plastic Very Very Thin (P-WFDSO), Ultra Thin (P-UFDSON), and Extremely Thin (P-XFDSO), Fine Pitch Dual Small Outline Non- Leaded Package Family (MO-252 Issue A, variation UAAD (6-ld)).

QFN: Plastic Very Very Thin (P-WFQFN), Ultra Thin (P-UFQFN), and Extremely Thin (P-XFQFN), Fine Pitch Quad Flat Small Outline, Non-Leaded Package Family (MO-255 Issue A, variation UAAD (8-ld), variation UABD (10-ld)).

3 Pinout standard

3.1 Description

The following criteria shall be used to convert existing 1-, 2- and 3-bit logic device functions offered in 5-, 6- and 8-pin DIP packages (e.g., SOP, SSOP, TSSOP) to 1-, 2- and 3-bit logic device functions offered in the 6- and 8-land SON/QFN packages:

- a) Attributes for the SON (6-ld) and QFN (8-ld) package package shall be as follows:
 - 6-land, 0.5-mm land pitch with 1.0-mm \times 1.45-mm body size and 3-row \times 2-column land array.
 - 8-land, 0.5-mm land pitch with 1.6-mm \times 1.6-mm body size and depopulated quad array.
- b) The pinout conversions shall be in accordance with the diagrams shown in sections 3.2 and 3.5. Each device shall be pinned out based on it's present package/pinout and the pinout tables in sections 3.3, 3.4, and 3.6.

3 Pinout standard (cont'd)

3.2 6-land SON package (MO-252, variation UAAD)

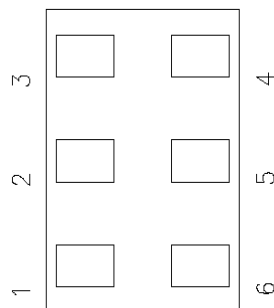


Figure 1 — Pinout configuration - Bottom view

3.3 Pin conversion from 5-pin DIP to 6-land SON package

The pinout adopts the naming convention of logic devices in 5-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 1 — 5-pin to 6-land pinout table

| Function (See Note) | Description | Pin Numbers | | | | | |
|------------------------|---|-----------------|-----|-----|----------------|-----|-----------------|
| | | 1 | 2 | 3 | 4 | 5 | 6 |
| 1G00 | Single 2-input NAND gate | A | B | GND | Y | DNU | V _{DD} |
| 1G02 | Single 2-input NOR gate | A | B | GND | Y | DNU | V _{DD} |
| 1G04 | Single inverter | DNU | A | GND | Y | DNU | V _{DD} |
| 1GU04 | Single unbuffered inverter | DNU | A | GND | Y | DNU | V _{DD} |
| 1G05 | Inverter with open-drain output | DNU | A | GND | Y | DNU | V _{DD} |
| 1G06 | Inverter with open-drain output | DNU | A | GND | Y | DNU | V _{DD} |
| 1G07 | Single buffer/driver with open-drain output | DNU | A | GND | Y | DNU | V _{DD} |
| 1G08 | Single 2-input AND gate | A | B | GND | Y | DNU | V _{DD} |
| 1G14 | Single inverter with Schmitt-trigger input | DNU | A | GND | Y | DNU | V _{DD} |
| 1G17 | Single buffer/driver with Schmitt-trigger input | DNU | A | GND | Y | DNU | V _{DD} |
| 1G32 | Single 2-input OR gate | A | B | GND | Y | DNU | V _{DD} |
| 1G34 | Single buffer | DNU | A | GND | Y | DNU | V _{DD} |
| 1G38 | Single 2-input NAND gate w/ open-drain output | A | B | GND | Y | DNU | V _{DD} |
| 1G66 | Single analog switch | I/O | I/O | GND | OE | DNU | V _{DD} |
| 1G79 | D-type flip-flop with Q output | D | CK | GND | Q | DNU | V _{DD} |
| 1G80 | D-type flip-flop with \overline{Q} output | D | CK | GND | \overline{Q} | DNU | V _{DD} |
| 1G86 | Single 2-input XOR gate | A | B | GND | Y | DNU | V _{DD} |
| 1G125 | Single buffer/driver with 3-state outputs | \overline{OE} | A | GND | Y | DNU | V _{DD} |
| 1G125 | Single bus switch | \overline{OE} | A | GND | B | DNU | V _{DD} |
| 1G126 | Single buffer/driver with 3-state outputs | OE | A | GND | Y | DNU | V _{DD} |

3 Pinout standard (cont'd)

Table 1 — 5-pin to 6-land pinout table

| Function (See Note) | Description | Pin Numbers | | | | | |
|------------------------|--------------------------------------|-----------------|---|-----|-----------------|-----|----------|
| | | 1 | 2 | 3 | 4 | 5 | 6 |
| 1G240 | Single inverter with 3-state outputs | \overline{OE} | A | GND | Y | DNU | V_{DD} |
| 1G384 | Single bus switch | A | B | GND | \overline{OE} | DNU | V_{DD} |

NOTE 1 The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

NOTE 2 DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

3.4 Pin conversion from 6-pin DIP to 6-land SON package

The pinout adopts the naming convention of logic devices in 6-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 2 — 6-pin to 6-land pinout table

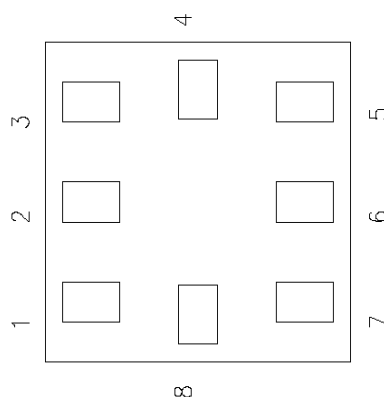
| Function | Description | Pin Numbers | | | | | |
|----------|--|-------------|-----|-----------------|----------------|----------|-----|
| | | 1 | 2 | 3 | 4 | 5 | 6 |
| 2G04 | Dual inverter | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 2GU04 | Dual unbuffered inverter | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 2G06 | Dual inverter with open-drain outputs | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 2G07 | Dual buffer/driver with open-drain outputs | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 1G10 | Single 3-input NAND gate | A | GND | B | Y | V_{DD} | C |
| 1G11 | Single 3-input AND gate | A | GND | B | Y | V_{DD} | C |
| 2G14 | Dual inverter with Schmitt-trigger inputs | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 2G16 | Dual buffer | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 2G17 | Dual buffer/driver with Schmitt-trigger inputs | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 1G18 | 1-of-2 non-inverting demux with 3-state output | S | GND | A | 1Y | V_{DD} | 0Y |
| 1G19 | 1-of-2 decoder/multiplexer | A | GND | \overline{OE} | 1Y | V_{DD} | 0Y |
| 1G27 | Single 3-input NOR | A | GND | B | Y | V_{DD} | C |
| 2G34 | Dual buffer/driver | 1A | GND | 2A | 2Y | V_{DD} | 1Y |
| 1G57 | Universal configurable 2-input gate | In1 | GND | In0 | Y | V_{DD} | In2 |
| 1G58 | Universal configurable 2-input gate | In1 | GND | In0 | Y | V_{DD} | In2 |
| 1G97 | Universal configurable 2-input gate | In1 | GND | In0 | Y | V_{DD} | In2 |
| 1G98 | Universal configurable 2-input gate | In1 | GND | In0 | Y | V_{DD} | In2 |
| 1G157 | Single 2-input non-inverting multiplexer | In1 | GND | In0 | Y | V_{DD} | S |
| 1G158 | Single 2-input inverting multiplexer | In1 | GND | In0 | \overline{Y} | V_{DD} | S |
| 1G175 | Single D-type flip-flop | CK | GND | D | Q | V_{DD} | CLR |
| 1G332 | Single 3-input OR | A | GND | B | Y | V_{DD} | C |

3 Pinout standard (cont'd)**Table 2 — 6-pin to 6-land pinout table**

| Function | Description | Pin Numbers | | | | | |
|----------|-------------------------------|-------------|-----|------|-----|-----------------|-----------------|
| | | 1 | 2 | 3 | 4 | 5 | 6 |
| 1G386 | Single 3-input XOR | A | GND | B | Y | V _{DD} | C |
| 1G373 | Single D-type latch | LE | GND | D | Q | V _{DD} | \overline{OE} |
| 1G374 | Single D-type flip-flop | CK | GND | D | Q | V _{DD} | \overline{OE} |
| 1G3157 | SPDT analog switch | I/O2 | GND | I/O1 | COM | V _{DD} | S |
| 1G3257 | 2-to-1 bus-switch multiplexer | B2 | GND | B1 | A | V _{DD} | S |

NOTE 1 The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

NOTE 2 DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

3.5 8-land QFN package (MO-255, variation UAAD)**Figure 2 — Pinout configuration - Bottom view****3.6 Pin conversion from 8-pin DIP to 8-land QFN package**

The pinout adopts the naming convention of logic devices in 8-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 3 — Generic conversion from 8-pin DIP package to 8-land QFN package

| Package Style | Pin numbers | | | | | | | |
|---------------|-------------|---|---|---|---|---|---|---|
| 8-pin DIP | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 8-land QFN | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 8 |

3 Pinout standard (cont'd)

Table 4 — 8-pin to 8-land pinout table

| Function | Description | Pin Numbers | | | | | | | |
|----------|--|--------------------------|-------------------------|------|-----|-------------------------|------|--------------------------|-----------------|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 2G00 | Dual 2-input NAND gate | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G02 | Dual 2-input NOR gate | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G08 | Dual 2-input AND gate | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G32 | Dual 2-input OR gate | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G38 | Dual 2-input NAND gate with open-drain output | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G53 | Dual analog MUX/DEMUX | I/O1 | I/O2 | S | GND | GND | INH | COM | V _{DD} |
| 2G66 | Dual analog switch | 1OE | 2I/O | 2I/O | GND | 2OE | 1I/O | 1I/O | V _{DD} |
| 2G74 | Single D-type flip-flop | $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | Q | GND | $\overline{\text{Q}}$ | D | CK | V _{DD} |
| 2G79 | Dual D-type flip-flop | 1Q | 2D | 2CK | GND | 2Q | 1D | 1CK | V _{DD} |
| 2G80 | Dual D-type flip-flop with inverting Q outputs | 1 $\overline{\text{Q}}$ | 2D | 2CK | GND | 2 $\overline{\text{Q}}$ | 1D | 1CK | V _{DD} |
| 2G86 | Dual 2-input XOR gate | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G125 | Dual buffer/driver with 3-state outputs | 2 $\overline{\text{OE}}$ | 1Y | 2A | GND | 2Y | 1A | 1 $\overline{\text{OE}}$ | V _{DD} |
| 2G126 | Dual buffer/driver with 3-state outputs | 2OE | 1Y | 2A | GND | 2Y | 1A | 1OE | V _{DD} |
| 2G132 | Dual 2-input NAND gate with schmitt-trigger inputs | 1Y | 2B | 2A | GND | 2Y | 1B | 1A | V _{DD} |
| 2G139 | Single 2-to-4 decoder | Y1 | Y2 | Y3 | GND | Y4 | B | A | V _{DD} |
| 2G157 | Single MUX/DEMUX | $\overline{\text{G}}$ | S | Y | GND | $\overline{\text{Y}}$ | B | A | V _{DD} |
| 2G240 | Dual inverting buffer with 3-state outputs | 2 $\overline{\text{OE}}$ | 1Y | 2A | GND | 2Y | 1A | 1 $\overline{\text{OE}}$ | V _{DD} |
| 2G241 | Dual buffer/driver with 3-state outputs | 2OE | 1Y | 2A | GND | 2Y | 1A | 1 $\overline{\text{OE}}$ | V _{DD} |
| 2G244 | Dual buffer/driver with 3-state outputs | 2 $\overline{\text{OE}}$ | 1Y | 2A | GND | 2Y | 1A | 1 $\overline{\text{OE}}$ | V _{DD} |
| 3G04 | Triple inverter | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3GU04 | Triple unbuffered inverter | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3G05 | Triple inverter with open-drain outputs | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3G06 | Triple inverter with open-drain outputs | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3G07 | Triple buffer/driver with open-drain outputs | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3G14 | Triple inverter with Schmitt-trigger inputs | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |

3 Pinout standard (cont'd)**Table 4 — 8-pin to 8-land pinout table**

| Function | Description | Pin Numbers | | | | | | | |
|----------|--|-------------|----|----|-----|----|----|----|-----------------|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 3G17 | Triple buffer/driver with Schmitt-trigger inputs | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |
| 3G34 | Triple buffer/driver | 1Y | 3A | 2Y | GND | 2A | 3Y | 1A | V _{DD} |

NOTE The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

NOTE DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Product*



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